Attorney: Craig A. Gelfound
Docket No.: 42112/CAG/B600
Inventor(s): Lawrence J. Madar, III et al
Title: PIPELINED MULTI-ACCESS MEMORY
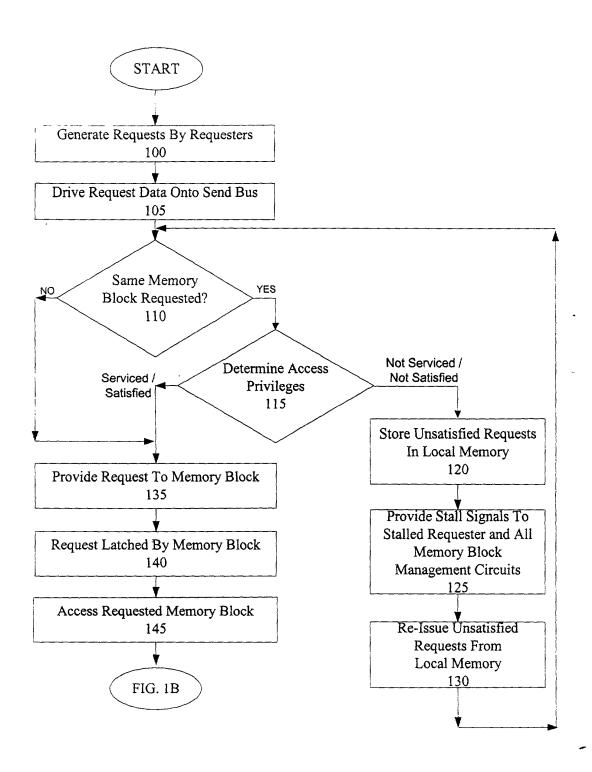APPARATUS AND METHOD
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FIG. 1A

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FIG. 1A

Read Request or Write Request? 150

Write Request

Read Request

Write Data To Memory Block 155

Lookup Read Data In Referenced Address 160

Drive Requested Data Onto Return Bus 170

Route Retrieved Data To Requester 175

Latch Retrieved Data Into Requester 180

END

FIG. 1B

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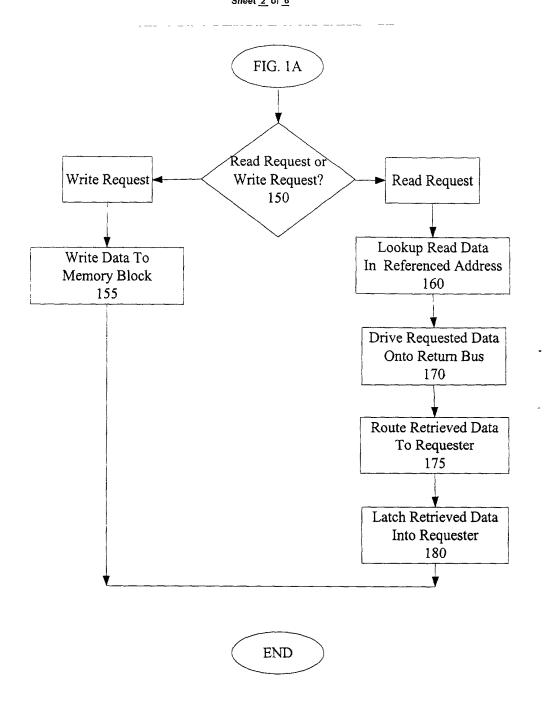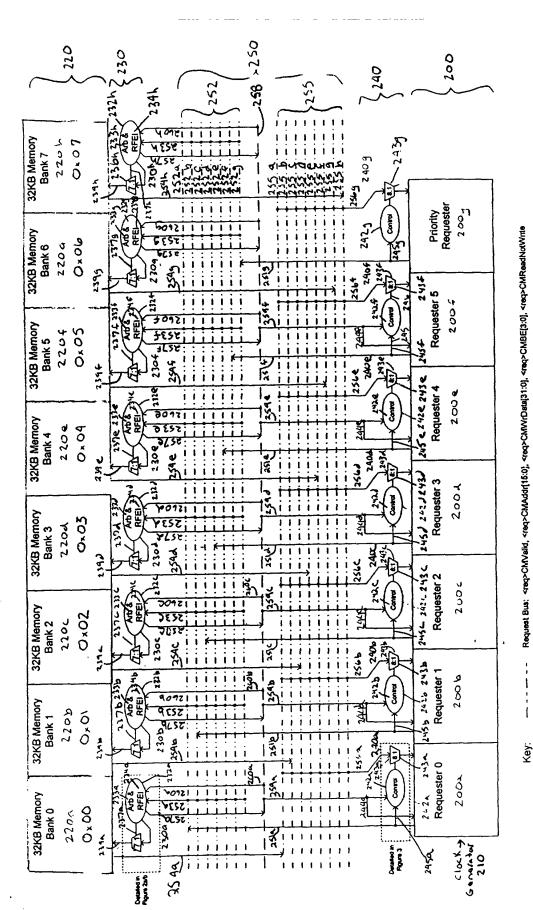APPARATUS AND METHOD
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Fig. 2

Key:

Request Bus: <req>CMValid, <req>CMAddr[15:0], <req>CMWrData[31:0], <req>CMBE[3:0], <req>CMReadNotWrite

Stall Busses: c<req>IntStall[7:0] (Eight lines per requester - one driven by each bank).

Data Return Bus: c<req>IntRdData[31:0]

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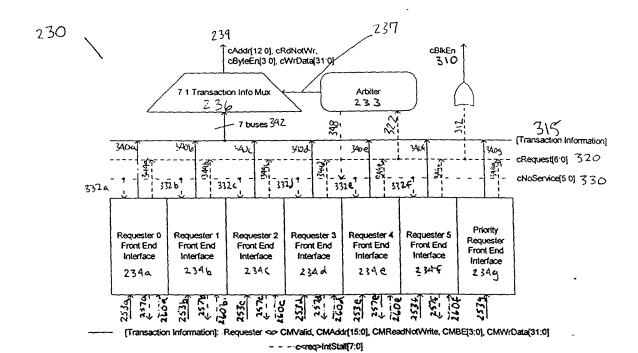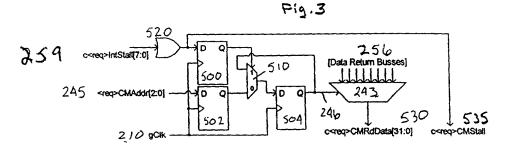Title: PIPELINED MULTI-ACCESS MEMORY
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230

239

237

cAddr[12 0], cRdNotWr,
cByteEn[3 0], cWrData[31 0]

cBlkEn
310

7 1 Transaction Info Mux
236

Arbiter
233

7 buses 342

348

322

312

315
[Transaction Information]

340a 340b 340c 340d 340e 340f 340g

cRequest[6 0] 320

344a 344b 344c 344d 344e 344f 344g

cNoService[5 0] 330

332a 332b 332c 332d 332e 332f

Requester 0 Front End Interface 234a	Requester 1 Front End Interface 234b	Requester 2 Front End Interface 234c	Requester 3 Front End Interface 234d	Requester 4 Front End Interface 234e	Requester 5 Front End Interface 234f	Priority Requester Front End Interface 234g

253a 257a 260a 253b 257b 260b 253c 257c 260c 253d 257d 260d 253e 257e 260e 253f 257f 260f 253g

——— [Transaction Information]: Requester <x> CMValid, CMAddr[15:0], CMReadNotWrite, CMBE[3:0], CMWrData[31:0]
– – – – c<req>IntStall[7:0]

Fig.3

259

520

c<req>IntStall[7:0]

D Q
500

510

256
[Data Return Busses]

243

245 <req>CMAddr[2:0]

D Q
502

D Q
504

246

530

535

210 gClk

c<req>CMRdData[31:0]

c<req>CMStall

Fig.5

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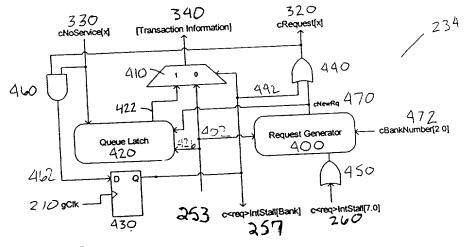Title: PIPELINED MULTI-ACCESS MEMORY
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330
cNoService[x]

340
[Transaction Information]

320
cRequest[x]

234

410

460

440

442

470
cNewRq

422

472
cBankNumber[2 0]

452

Queue Latch
420

Request Generator
400

431b

462

D   Q

210 gClk

450

430

253

c<req>IntStall[Bank]
257

c<req>IntStall[7 0]
260

Fig. 4

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FIG. 6